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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,650	07/15/2003	Hiroshi Kondoh	240266US2	5255

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

G.a.

Office Action Summary	Application No.	Applicant(s)	
	10/618,650	KONDOH, HIROSHI	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-46* is/are pending in the application.

4a) Of the above claim(s) *8-17,27 and 28* is/are withdrawn from consideration.

5)☒ Claim(s) *3,29,30 and 33 -46* is/are allowed.

6)☒ Claim(s) *1,2,5-7,18-23,26,31 and 32* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 21, 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1, 2, 5, 6** and **7** are rejected under 35 U.S.C. 102(b) as being anticipated by Dodabalapur et al. (US Patent no. 6,278127).

4. Regarding claim **1**, Dodabalapur discloses a semiconductor device, comprising: a gate electrode 14 (fig. 2);

an insulating layer 15 (fig. 2) on the gate electrode 14; a first electrode 12 (fig. 2) on the insulating layer 15; a second electrode 13 (fig. 2) on the insulating layer 15 at an interval with the first electrode 12;

an organic semiconductor layer 16 (fig. 2) disposed in the interval between the first electrode 12 and the second electrode 13 and covering at least part of the first electrode and the second electrode; and

a first resistance layer 21 (fig. 2) is n-type (e.g.,Alq; column 5, lines 12 – 13) formed on the organic semiconductor layer 16and having an electrical resistance lower than an electrical resistance of the organic semiconductor layer (fig. 9; column 5, lines 53 – 54).

Regarding claim **2**, Dodabalapur discloses both a distance (50 nm as the thickness of organic semiconductor) from the first electrode to the first resistance layer and a distance from the second electrode to the first resistance layer are shorter than the interval between the first electrode and the second electrode (12 micrometers; column 5, lines 60 – 64).).

Regarding claim **5**, Dodabalapur discloses the first electrode 12, the second electrode 13 and the first resistance layer 21 is in contact with the organic semiconductor layer 16; and an interface between one of the first electrode, the second electrode and the first resistance layer rectifies an electrical current therethrough (col. 5, lines 1 – 46).

Regarding claim **6**, Dodabalapur discloses the resistance layer 21 is formed to be a plate shape (broadly interpreted; fig. 2).

Regarding claim **7**, Dodabalapur discloses a substrate 11 (fig. 2) is beneath the gate electrode 14 (fig. 2).

Regarding claim **18**, Dodabalapur discloses the organic semiconductor layer is formed from thiopene derivatives (column 3, lines 14 – 44).

Regarding claim **21**, Dodabalapur discloses each of the first electrode, the second electrode, and the gate electrode is formed from gold (column 2, lines 53 – 57; column 3, lines 1 and 2; and column 5, lines 59 – 62).

Regarding claim **22**, Dodabalapur discloses the insulating layer is formed from conventionally SiO_2 (column 5, lines 61 – 62).

Regarding claim **23**, Dodabalapur discloses the claimed invention of claim 1 except for the insulating layer is formed from at least a metal oxide film produced by coating and baking a solution obtained via hydrolysis of a metal alkoxide represented by one of the general formulas M(OR).sub.n and MR(OR').sub.n-1, wherein each of R and R' is an organic group such as an alkyl group and a phenyl group, M is a metal in one of IVA through VIIA groups, VIII group, and IB through VIB groups of the periodic table, and n is an ionic valence of the metal M. However this limitation is taken to be a product by process limitation, it is the patentability product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear

that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claims **31** and **32**, Dodabalapur discloses a gate dielectric layer conventionally formed SiO_2 (column 5, lines 61 – 62).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim **26** is rejected under 35 U.S.C. 103(a) as being unpatentable over Dodabalapur et al. (US Patent no. 6,278,127) in view of Yang et al. (US Patent Application Publication no. 2002/013555).

7. Regarding claim **26**, Dodabalapur discloses the claimed invention of claim 1 except for a first power supply conducting a current between the first electrode and the second electrode; and a second power supply applying a voltage to the gate electrode.

However, it is conventional and also taught by Yang that transistor having a power supply to the gate of M7 (fig. 4) and a power supply connected to source (first electrode) and drain (second electrode).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a first power supply conducting a current between the first electrode and the second electrode; and a second power supply applying a voltage to the gate electrode in order to be able to program the device.

Allowable Subject Matter

8. Claims **3, 29, 30** and **33 – 46** are allowed.

9. The following is an examiner's statement of reasons for allowance: Claims **3, 29, 30** and **33 – 45** are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

a first resistance layer 6 (fig. 6) being contacted with one of the first electrode 3 (fig. 6) and the second electrode as cited in the independent claims 3, 29 and 30; a second resistance layer 7 (fig. 30) formed at least one of the position between the first resistance layer 6 (fig. 30) and the organic layer 5 (fig. 30), the position between the first electrode 3 (figs. 8 & 9) and the organic semiconductor layer 5 (fig. 9); and position between second electrode 4 (fig.10) and the organic semiconductor layer 5 (fig. 10) and carriers in the organic semiconductor layer allowed to tunnel through the second resistance layer when a voltage equal or more than a voltage of predetermined value being applied across the second resistance layer as cited in the independent claim 46; and among other limitations as cited in the independent claims 3, 29, 30 and 46.

10. Claim **4** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is an examiner's statement of reasons for the indication of allowable subject matter: Claim **4** is allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

A second resistance layer 7 (fig. 30) formed at least one of the position between the first resistance layer 6 (fig. 30) and the organic layer 5 (fig. 30), the position between the first electrode 3 (figs. 8 & 9) and the organic semiconductor layer 5 (fig. 9); and position between second electrode 4 (fig.10) and the organic semiconductor layer 5 (fig. 10).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

January 2, 2006